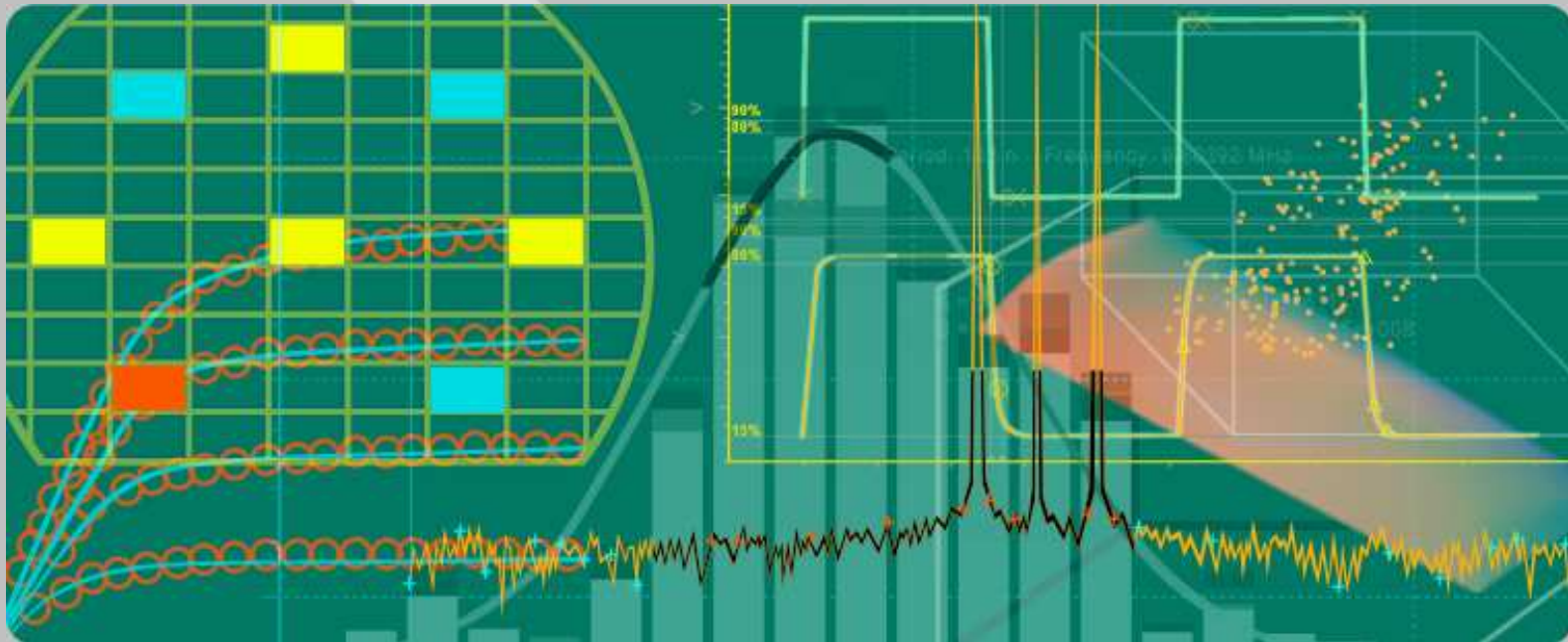


# UTMOST IV SPICE Optimization Module

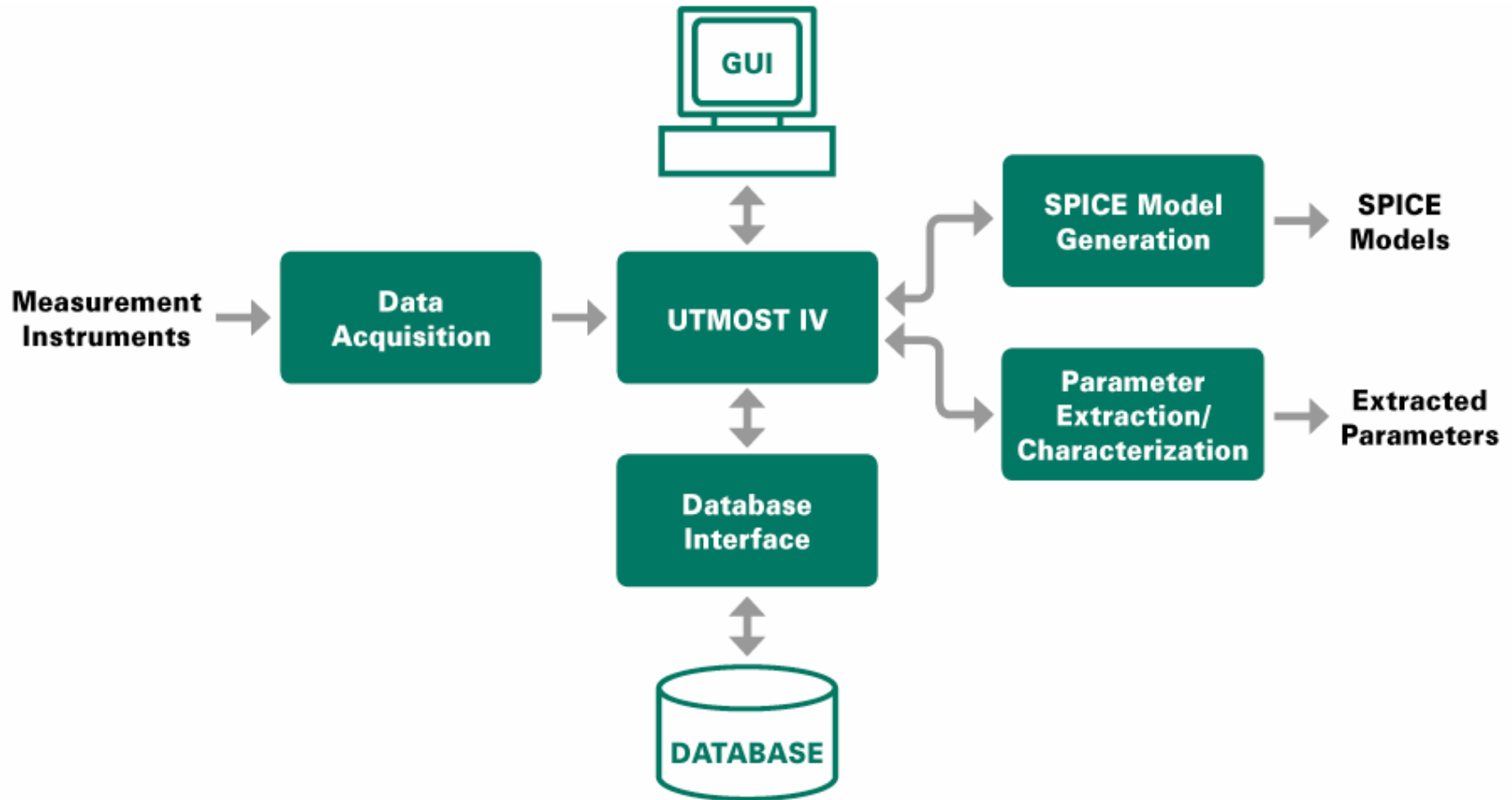


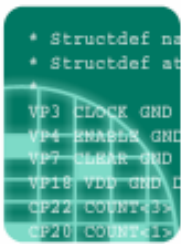
Dr. Ivan Pestic

January 2007

```
* Structdef na
* Structdef at
VP3 CLOCK GND
VP4 ENABLE GND
VP7 CLEAR GND
VP18 VDD GND
CP22 COUNT<3>
CP20 COUNT<1>
```

# UTMOST IV Architecture



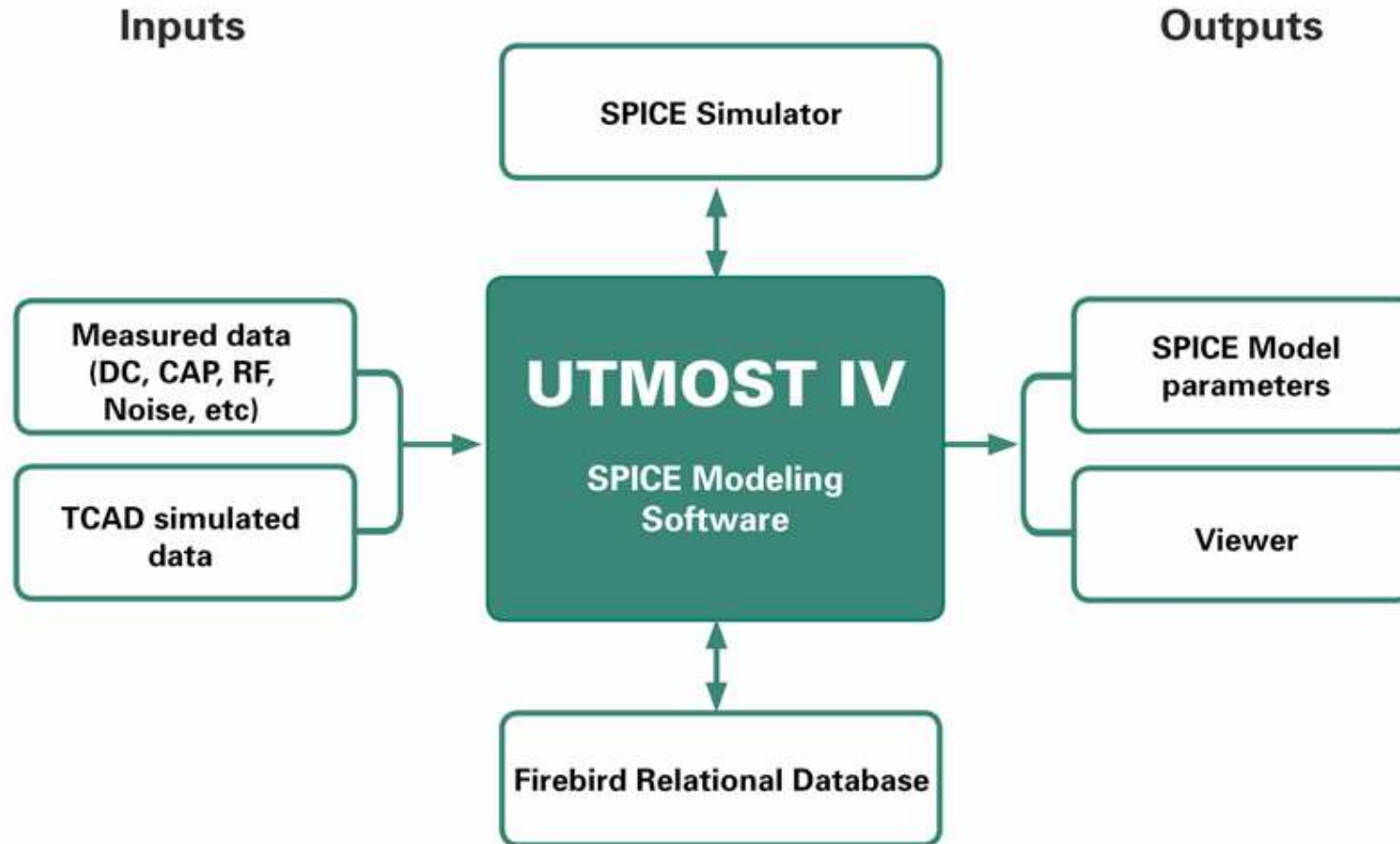


# Optimization Module Overview

- Underlying 64-bit Relational Database
- Flexible Data Format
- Technology Independent
- Full Macro-model Support
- High-speed SmartSpice Interface
- Unlimited Multi-target Optimization
- Family of Advanced Optimizers

```
* Structdef na
* Structdef at
VP3 CLOCK GND
VP4 ENABLE GND
VP7 CLEAR GND
VP18 VDD GND
CP22 COUNT<3>
CP20 COUNT<1>
```

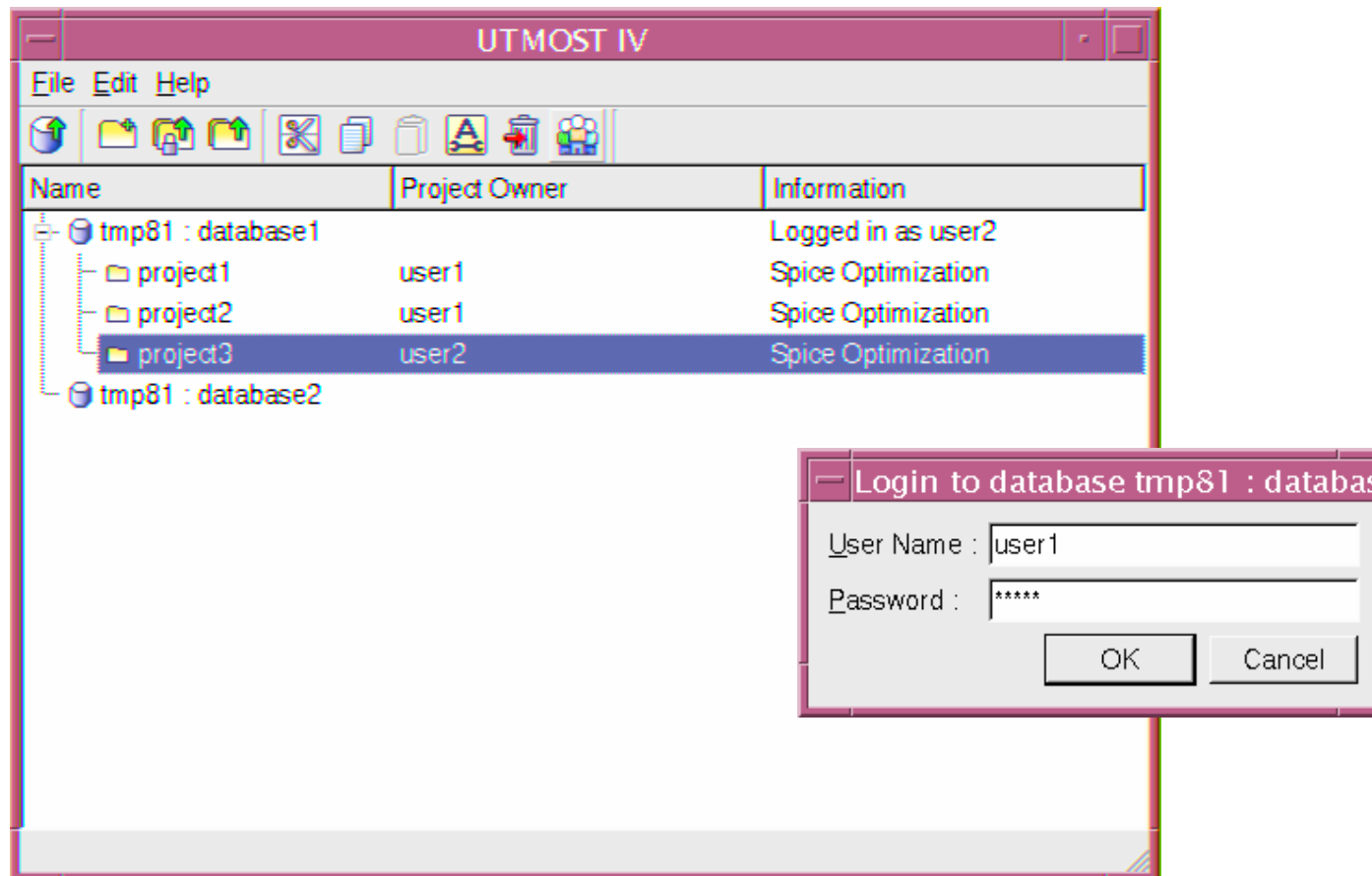
# UTMOST IV Optimization Module Architecture



```
* Structdef na
* Structdef at
VP3 CLOCK GND
VP4 ENABLE GND
VP7 CLEAR GND
VP18 VDD GND
CP22 COUNT<3>
CP20 COUNT<1>
```

# 64-bit Relational Database

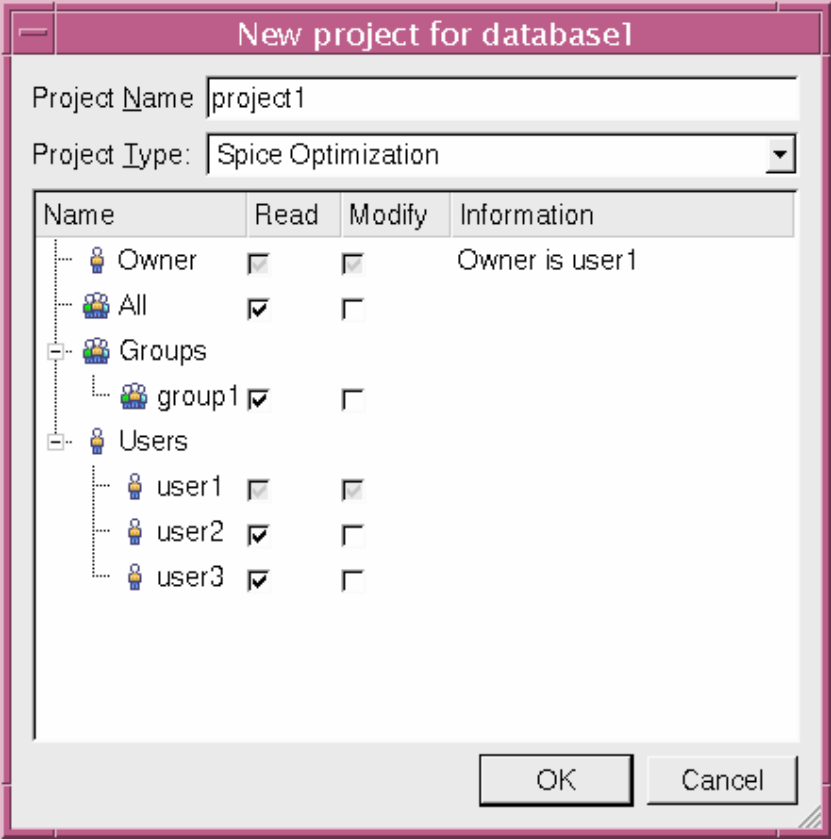
- Multi-user, multi-access Firebird 64bit relational database organises your work
- Data sharing, storage and retrieval



```
* Structdef na
* Structdef at
VP3 CLOCK GND
VP4 ENABLE GND
VP7 CLEAR GND
VP18 VDD GND
CP22 COUNT<3>
CP20 COUNT<1>
```

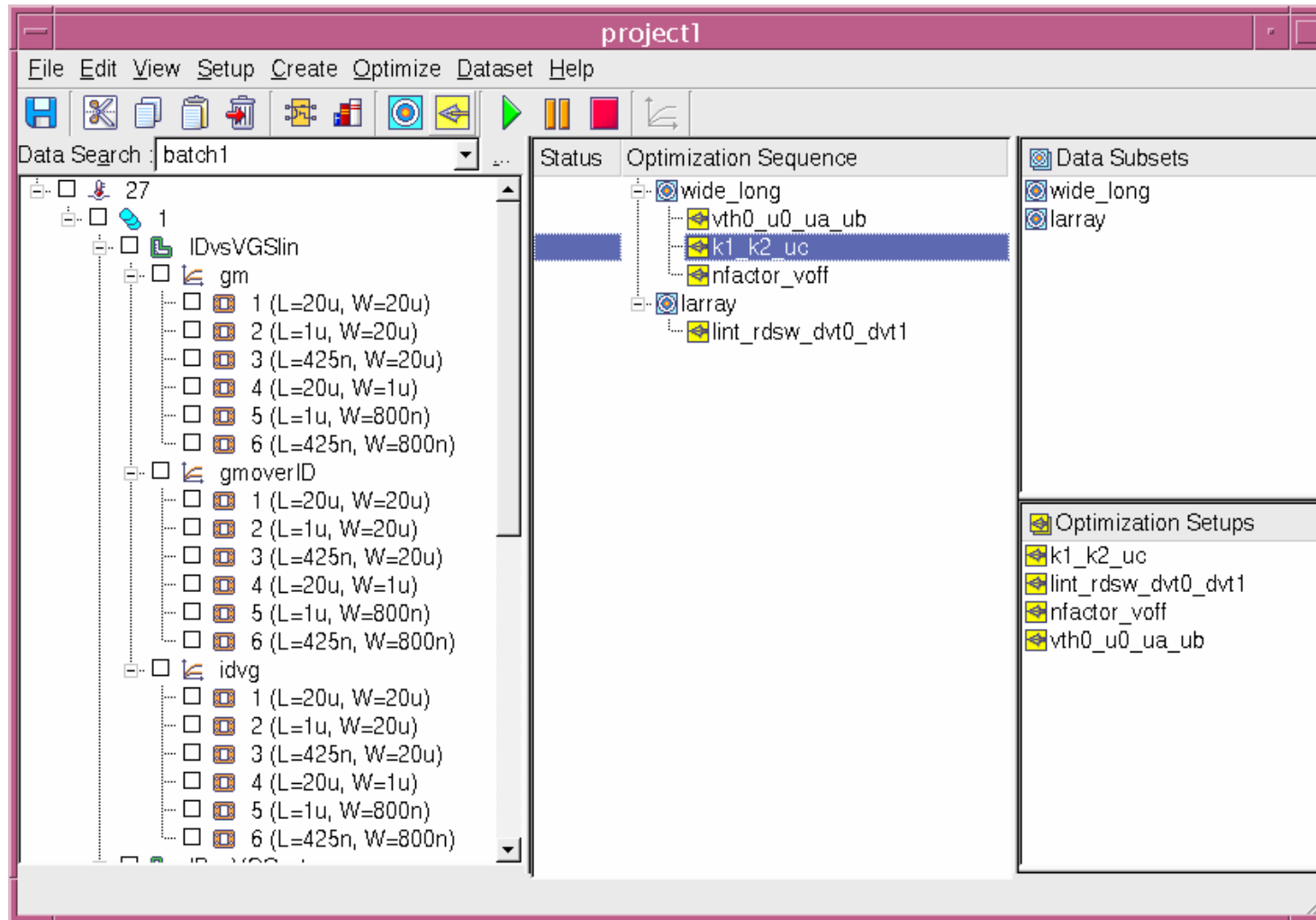
# Database Permissions

- Full access control for data security



```
* Structdef na
* Structdef at
VP3 CLOCK_GND
VP4 ENABLE_GND
VP7 CLEAR_GND
VP18 VDD_GND
CP22 COUNT<3>
CP20 COUNT<1>
```

# The Project Window

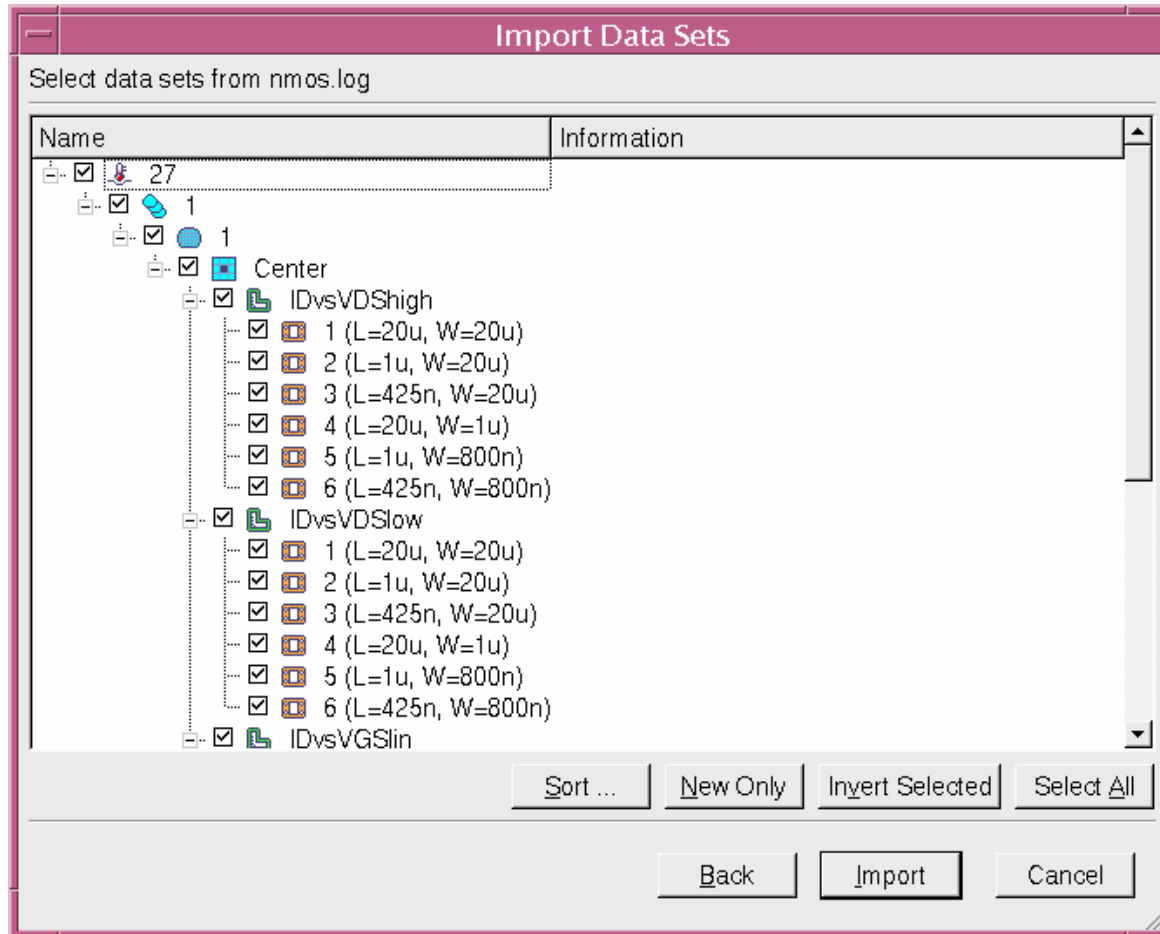


```

* Structdef na
* Structdef at
VP3 CLOCK GND
VP4 ENABLE GND
VP7 CLEAR GND
VP18 VDD GND
CP22 COUNT<3>
CP20 COUNT<1>

```

# Data Import



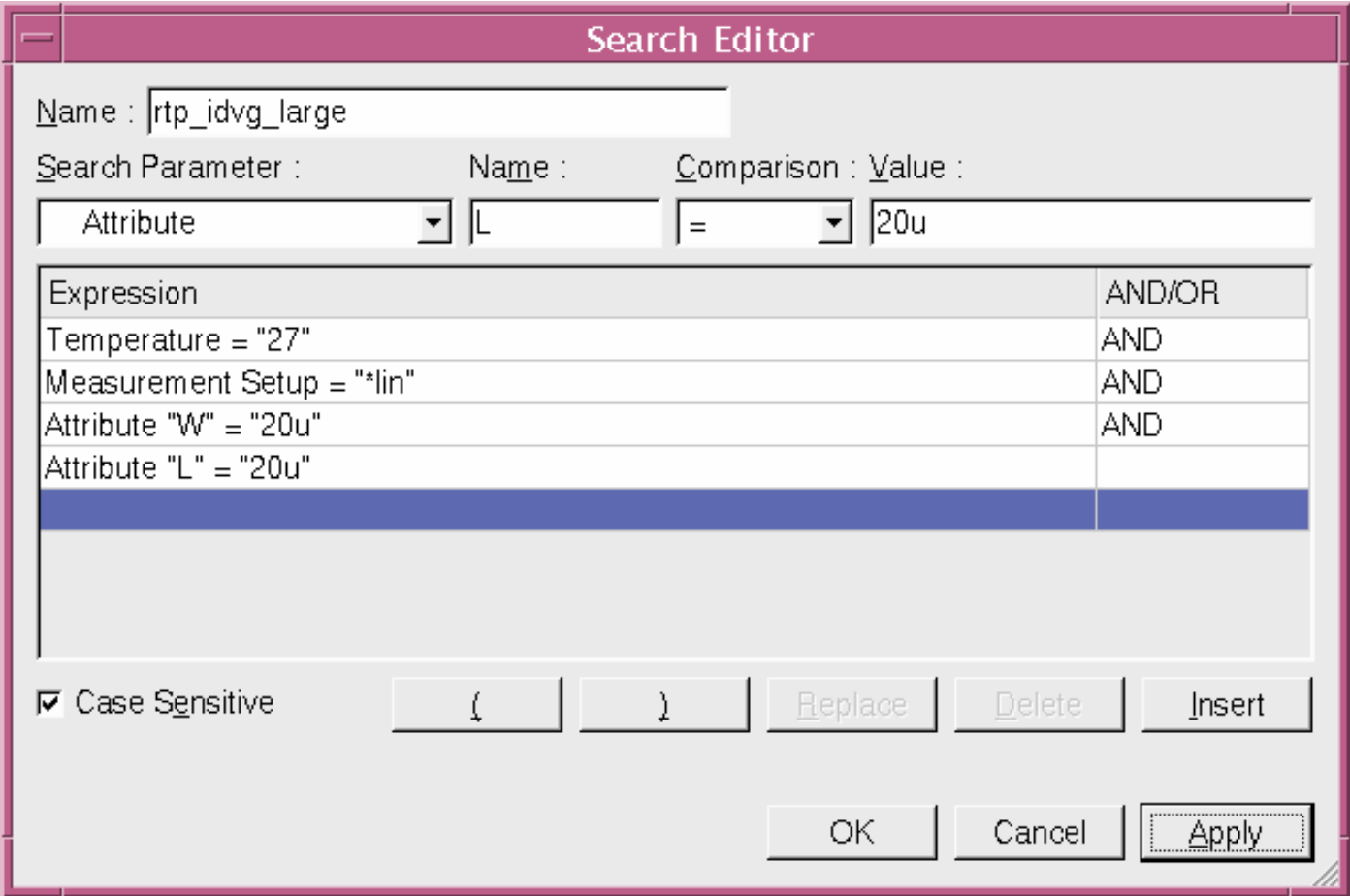
- Dataset import for legacy UTMOST III logfiles
- Flexible dataset import using UTMOST IV datafiles
- No longer any requirement for data to have equally spaced points
- Sweeps can be linear or logarithmic, or simply a list of values

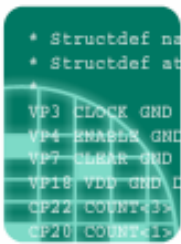


```
* Structdef na
* Structdef at
VP3 CLOCK GND
VP4 ENABLE GND
VP7 CLEAR GND
VP18 VDD GND
CP22 COUNT<3>
CP20 COUNT<1>
```

# Search Editor

- Database search allows you to retrieve and share information





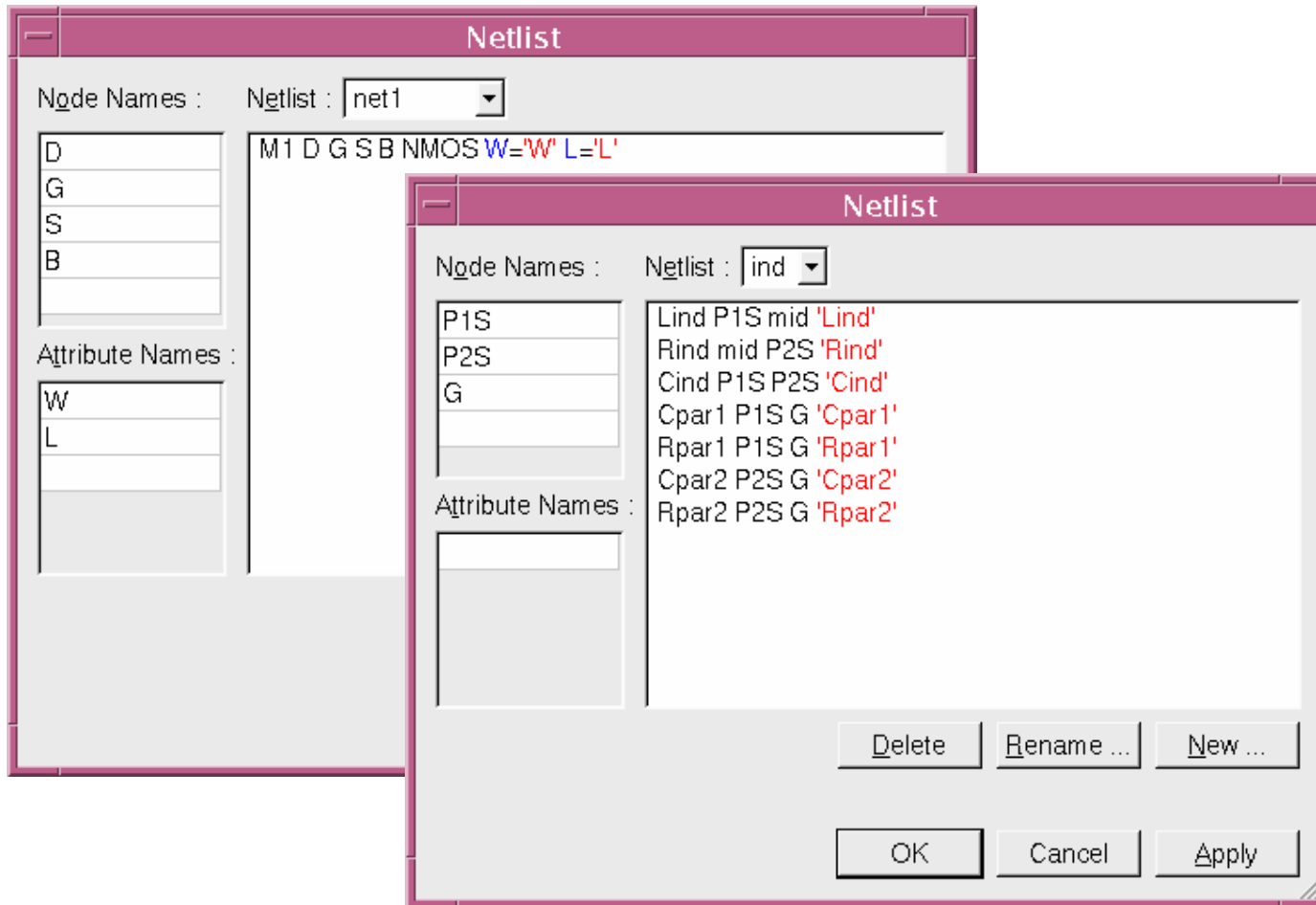
## Technology Independent

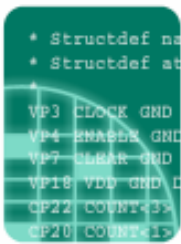
- No more BIP, MOS, SOI, SPICE model modules to buy like in UTMOST III and competitors' software
- No limit to number of name of device nodes
- Supports all types of semiconductor devices
- All spice model types available through SmartSpice

```
* Structdef na
* Structdef at
VP3 CLOCK GND
VP4 ENABLE GND
VP7 CLEAR GND
VP18 VDD GND
CP22 COUNT<3>
CP20 COUNT<1>
```

# Netlist Definition

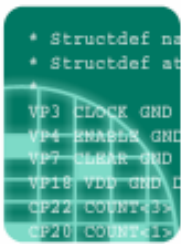
- Netlist of any complexity can be defined for macro-model
- All macro-model parameters available for simultaneous optimization and rubberbanding





# High Speed SmartSpice Interface

- Simulation is provided using the full power and flexibility of SmartSpice
- Very fast simulation times provided by high speed API interface
  - 80 dc simulations per second on AMD Atlon64 X2 4800
- No significant loss in speed when using macro-model instead of compact model
- Optimization time for typical LDMOS macro-model
  - UTMOST III approx. 1.5 - 2.0 hours
  - **UTMOST IV approx. 2-3 minutes**



## ModelLib Saves the Day

- UTMOST IV no longer contains the models
- Model information provided by ModelLib in SmartSpice
- No difference between SPICE simulator and model extractor is possible
- Any new SPICE models in SmartSpice are also instantly available to UTMOST IV
- Web-based and web-delivered model updates

```

* Structdef na
* Structdef at
VP3 CLOCK GND
VP4 ENABLE GND
VP7 CLEAR GND
VP18 VDD GND
CP22 COUNT<3>
CP20 COUNT<15>

```

# Model Library

- No limit to number or type of models
- Versatile import and export

Model Library : project1

Model Parameter Simulation

Model Name :  Type : NMOS 0 marked. Find :

	Mark	Name	Optimized	Fit Initial	User Initial	Minimum	Maximum
1	<input checked="" type="checkbox"/>	LEVEL	8	8	8		
2	<input type="checkbox"/>	VERSION	3.3	3.3	3.3	3	3.3
3	<input type="checkbox"/>	TNOM	27	27	27	-100	300
4	<input type="checkbox"/>	TOX	14n	14n	14n	5n	50n
5	<input type="checkbox"/>	XJ	150n	150n	150n	100n	1u
6	<input type="checkbox"/>	NCH	1.7e+17	1.7e+17	1.7e+17	5e+16	5e+17
7	<input type="checkbox"/>	NSUB				5e+15	3e+17
8	<input type="checkbox"/>	VTH0	700m	700m	700m	-2	2
9	<input type="checkbox"/>	K1	500m	500m	500m	0	1
10	<input type="checkbox"/>	K2	-18.6m	-18.6m	-18.6m	-50m	0
11	<input type="checkbox"/>	K3	80	80	80	1m	100
12	<input type="checkbox"/>	K3B	0	0	0	-10	10
13	<input type="checkbox"/>	W0	2.5u	2.5u	2.5u	1u	10u
14	<input type="checkbox"/>	NLX	174n	174n	174n	10n	1u
15	<input type="checkbox"/>	DVT0W	0	0	0	-500m	500m
16	<input type="checkbox"/>	DVT1W	0	0	0	0	10M
17	<input type="checkbox"/>	DVT2W	0	0	0	500m	500m

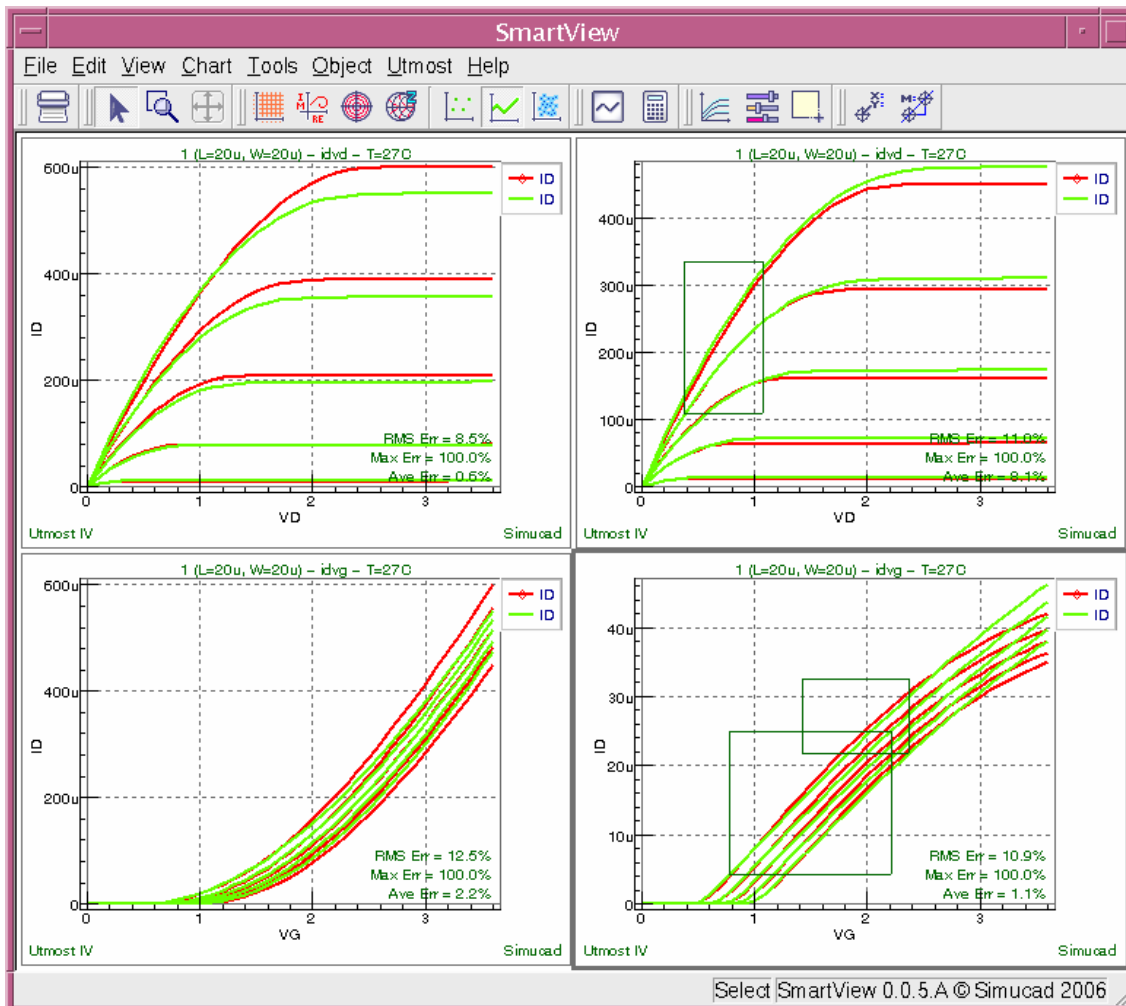
```

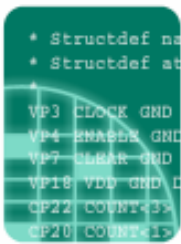
* Structdef na
* Structdef at
VP3 CLOCK GND
VP4 ENABLE GND
VP7 CLEAR GND
VP18 VDD GND
CP22 COUNT<3>
CP20 COUNT<1>

```

# Multi-target Optimization

- Any combination of data can be used as the target for an optimization
- Multiple temperatures, mix dc and ac, multiple batch or wafers





# Family of Advanced Optimization Algorithms

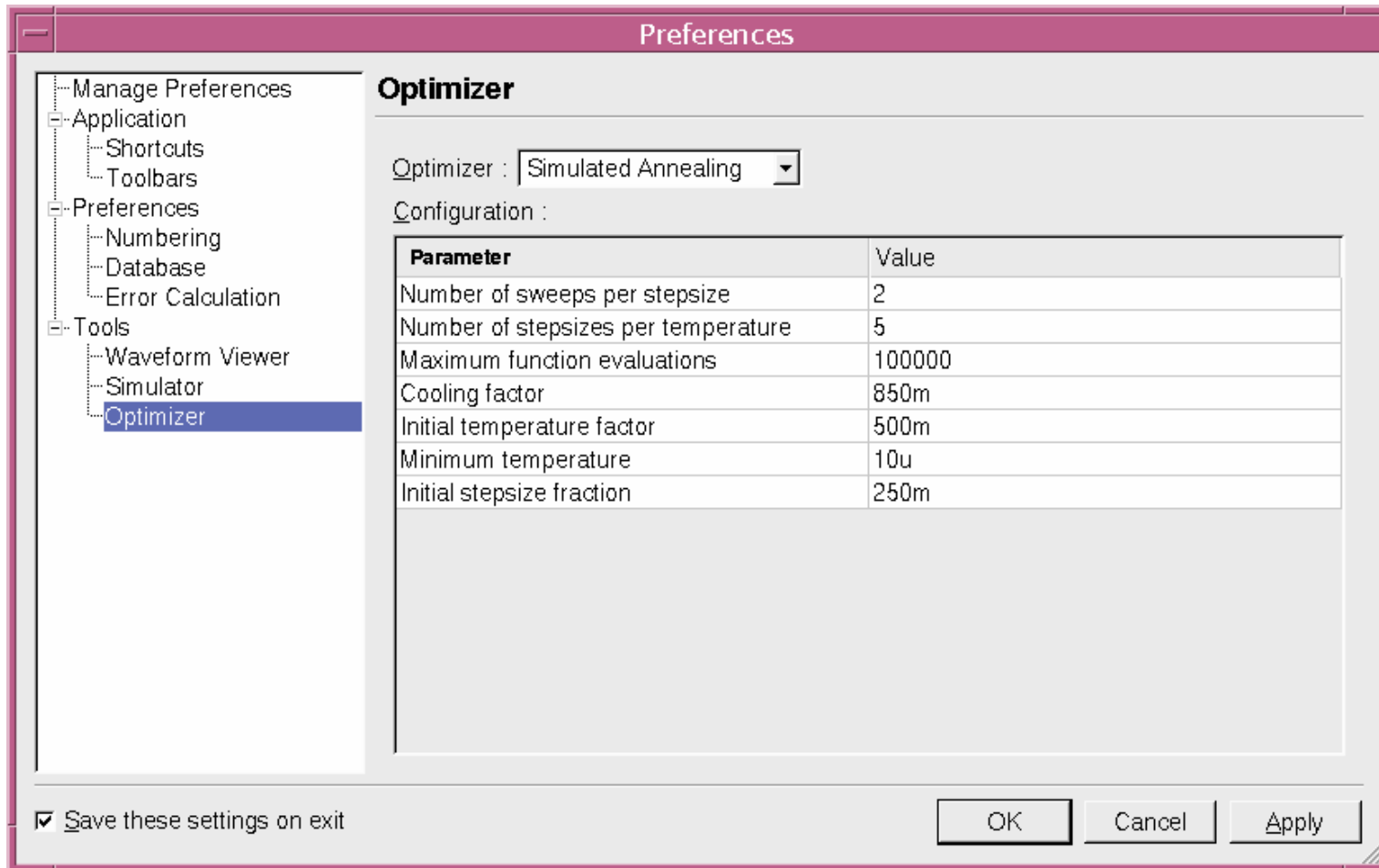
- Local (traditional) optimizers are fast, but need good starting point
  - Levenberg Marquartz
  - Gauss-Siedel
  - Hooke-Jeeves
- Global (next generation) optimizers run more iterations, but require less conditioning
  - Genetic Algorithm
  - Simulated Annealing
  - Parallel Tempering
  - Differential Evolution



```
* Structdef na
* Structdef at
VP3 CLOCK GND
VP4 ENABLE GND
VP7 CLEAR GND
VP18 VDD GND
CP22 COUNT<3>
CP20 COUNT<1>
```

# Optimizer Settings

- Easy to select and configure optimizer



```
* Structdef na
* Structdef at
VP3 CLOCK GND
VP4 ENABLE GND
VP7 CLEAR GND
VP18 VDD GND
CP22 COUNT<3>
CP20 COUNT<1>
```

# Rubberband Optimization

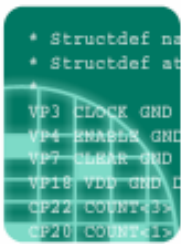
- No limit to number of parameters
- Parameters for multiple models may be optimized at the same time

Parameter Optimization

Model : nmos      Optimized Parameters :      Iteration : 207    Error = 4.0%

Model/Parameter	Value	Minimum	Maximum
nmos/TOX	7.3043n	5n	50n
nmos/VTH0	444.98m	-2	2
nmos/K1	639.28m	0	1
nmos/K2	-21.136u	-19	14.901n
nmos/K3	100	1m	100
nmos/U0	40.697m	10m	100m
nmos/UA	100p	100p	10n
nmos/UB	8.9745e-19	1e-21	5a
nmos/UC	45.958p	-100p	10n

Buttons: Revert, Optimize, OK, Cancel, Apply



## Conclusion

- UTMOST IV Optimization Module provides an easy to use, database-driven environment for the generation of accurate, high quality SPICE models and macro-models for analog, mixed-signal and RF applications
- UTMOST IV provides model extraction solution for problems that were not possible to solve with UTMOST III and competitors' software
  - Deep sub-micron CMOS with the new generation of SPICE models (HiSIM, PSP, Dual Gate, BSIM, etc.)
  - Complex power MOS/Bipolar macro-models
  - Passive and active RF macro-model (varactor, inductor, etc.) s-parameter optimization